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DINSMORE & SHOHL LLP			ALSIP, MICHAEL	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/591,922	Applicant(s) JALOWIECKI ET AL.
	Examiner MICHAEL ALSIP	Art Unit 2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 19 October 2010.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-6 and 8-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-6 and 8-25 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO/GS-68)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____

5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-6, 8-10, 12-19 and 24-25** are rejected under 35 U.S.C. 102(b) as being anticipated by Baddiley (US 4,852,065).

3. Consider **claim 1**, Baddiley discloses a multi-ported orthogonal data memory for effecting a corner-turning function, where for example data input as a sequence of bit-parallel word-serial data transfers are converted to data output in a bit-serial, word-parallel fashion; the memory being arranged to transfer data words comprising a plurality of data items (fig. 2, abstract, Col. 1 lines 4-30 and Col. 3 lines 20-50, where a data item is considered to be a data word or some portion of a data word.) and comprising: a plurality of data memory cells arranged in the form of a matrix having rows and columns, and a plurality of groups of memory cells within the matrix, **wherein each group is defined across multiple rows and columns, wherein each group relates to a different size of data item and wherein each group is individually addressable to effect transfer of a data word thereto** (fig. 2, Col. 3 lines 20-58 and Col. 5 lines 1-10, where a group of memory cells can be each buffer 20 and 21 themselves or a subset of a buffer that spans multiple rows and columns and the word data that is stored in each

buffer and thus each group can be used to handle words of 32-bit size or smaller based on preset values and therefore each group is related to data items of a different size.); and enabling means having dedicated strobe connections to each of the plurality of groups of memory cells and being arranged to enable selected ones of the plurality of groups of memory cells, **as determined by the size of the data items being transferred**, to read data present at their inputs or to write stored data to their outputs in a single transfer operation (Fig. 2 and 3, Col. 3 lines 20-58 and Col. 5 lines 1-10, where each buffer is selected after a determination of the size of the data items is made and the arrangement of the data in the buffer is effected by the word size. Each buffer has dedicated connections for reading out and writing in data as shown in fig. 2 and 3 and a write or read operation is considered a single transfer operation.).

4. Consider **claim 2**, Baddiley discloses a memory according to **Claim 1**, wherein each of the groups of memory cells is specified according to its use in transferring the data items of the data word to or from the matrix to effect the corner-turning function (Col. 3 lines 20-58, each buffer is designated to either be a write or read buffer).

5. Consider **claim 3**, Baddiley discloses a memory according to **Claim 1**, wherein the enabling means comprises selection means for selecting the current size of the data items in the data word and configuring the enabling means to operate with the selected current size of data items (Col. 5 lines 1-10, where the size of the data items in the word is considered the size of the data items together that make up the whole word).

6. Consider **claim 4**, Baddiley discloses a memory according to **Claim 3**, wherein the number of different groups of memory cells provided within the matrix equals the

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number of different sizes of data items which can be handled by the memory (Fig. 2, col. 3 lines 20-50 and Col. 5 lines 1-10, where a group of memory cells can be considered any subset of memory cells of a buffer that spans multiple rows and columns and word sizes of 32 bits or lower can be used by the system, therefore since a group is merely defined as spanning multiple rows and columns, the number of groups can be equal to the number of sizes available).

7. Consider **claim 5**, Baddiley discloses a memory according to **Claim 3**, wherein each item of the data word being transferred is an integer power-of-two multiple of eight bits (Col. 5 lines 1-10).

8. Consider **claim 6**, Baddiley discloses a memory according to **Claim 1**, wherein the memory is arranged to operate with different types of data words, each type comprising 64, 32, 16 or 8-bit data items (Col. 5 lines 1-10).

9. Consider **claim 8**, Baddiley discloses a memory according to **Claim 7**, wherein the enabling means is arranged to enable a selected group upon a set of logic conditions becoming true, the logic conditions being determined from a current selected row of the matrix and the size of the items being transferred (fig. 2 and 4, Col. 3 lines 20-59 and Col. 5 lines 1-10, where logic conditions include the decoder using the control and address bits to select particular rows or columns in a particular buffer).

10. Consider **claim 9**, Baddiley discloses a memory according to **Claim 1**, wherein the enabling means comprises a pointer in a shift register (38) for determining which rows of the matrix are to be enabled for taking part in the data transfer of all of the data items of the data word (Fig. 4, Col. 3 lines 50-59, Col. 4 lines 33-37, where register 45

comprises a reference to counter 40 and is used in determining the control and address bits to enable particular rows of the matrix).

11. Consider **claim 10**, Baddiley discloses a memory according to **Claim 9**, wherein the pointer in the shift register (38) is configured to be operable in a plurality of different modes , each mode corresponding to a possible size of the data item being transferred, the pointer being configured within a single instruction to advance by a predetermined number of bit positions as determined by the current mode thereby indicating which rows of the matrix are to be enabled to facilitate transfer of the whole of the data word to or from the matrix (fig. 4, Col. 3 lines 30-59, col. 4 lines 33-37 and Col. 5 lines 1-10, where register 45 determines word size and address and control bits to indicate rows and columns of a matrix to facilitate transfer of data words).

12. Consider **claim 12**, Baddiley discloses a memory according to **Claim 9**, further comprising means for converting the current position of the row pointer in the shift register (38) to one or more row select logic signals (Fig. 4, Col. 3 lines 50-59, Col. 4 lines 33-37, where register 45 comprises a reference to counter 40 and is used in determining the control and address bits to enable particular rows of the matrix).

13. Consider **claim 13**, Baddiley discloses a memory according to **Claim 12**, further comprising a hard-wired backward propagation network for determining, from the bit position of the pointer and the size of the current data items, the rows of the matrix that are to be enabled for the data transfer (Fig. 4, Col. 3 lines 50-59, Col. 4 lines 33-37, where register 45 comprises a reference to counter 40 and is used in determining the control and address bits to enable particular rows of the matrix, the components of fig. 4

perform the functions claimed to be performed by the hard-wired backward propagation network).

14. Consider **claim 14**, Baddiley discloses a memory according to **Claim 1**, wherein the enabling means comprises byte column determining means for enabling a specific group of byte column locations of the matrix within a selected word row to be enabled for transferring an item of the data word across a word port of the memory (Fig. 3-4 Col. 4 lines 6-46 and Col. 5 lines 45-62, where register 46 comprises a reference to counter 41 and is used in determining the control and address bits to enable particular columns of the matrix and 43 determines which buffer is being referenced by which register/counter combination).

15. Consider **claim 15**, Baddiley discloses a memory according to **Claim 14**, wherein the byte column determining means comprises a table specifying the relationship between the plurality of different groups of memory cells and their respective memory cell locations in the matrix (fig. 3-4, Col. 3-4 lines 29-41 and 59-33 and Col. 5 lines 45-62, where register's 40 and 41 consist of a linear table of bits with indicate a particular row/column for reading or writing information in a particular buffer).

16. Consider **claim 16**, Baddiley discloses a memory according to **Claim 1**, wherein the enabling means comprises bit column determining means for enabling a specific group of bit column locations of the matrix within a selected word row to be enabled for transferring a bit of an item of the data word across a bit port of the memory (Fig. 3-4 Col. 4 lines 6-46 and Col. 5 lines 45-62, where register 46 comprises a reference to counter 41 and is used in determining the control and address bits to enable particular

columns of the matrix and 43 determines which buffer is being referenced by which register/counter combination).

17. Consider **claim 17**, Baddiley discloses a memory according to **Claim 16**, wherein the bit column determining means comprises a table specifying the relationship between the plurality of different groups of memory cells and their respective memory cell locations in the matrix (fig. 3-4, Col. 3-4 lines 29-41 and 59-33 and Col. 5 lines 45-62, where register's 40 and 41 consist of a linear table of bits with indicate a particular row/column for reading or writing information in a particular buffer).

18. Consider **claim 18**, Baddiley discloses a memory according to **Claim 1**, wherein the locations of the memory cells of each group form a repeating pattern when viewed as a matrix (fig. 2).

19. Consider **claim 19**, Baddiley discloses a memory according to **Claim 1**, further comprising a load register (42) arranged to retain temporarily bit-serial word parallel data transferred to and from the matrix of memory cells across a bit port of the memory (Fig. 3 and Col. 4 lines 20-25).

20. Consider **claim 24**, Baddiley discloses a memory according to **Claim 2**, wherein the enabling means comprises selection means for selecting the current size of the data items in the data word and configuring the enabling means to operate with the selected current size of data items (Col. 5 lines 1-10, where the size of the data items in the word is considered the size of the data items together that make up the whole word).

21. Consider **claim 25**, Baddiley discloses a memory according to **Claim 3**, wherein the enabling means comprises a pointer in a shift register (38) for determining which

rows of the matrix are to be enabled for taking part in the data transfer of all of the data items of the data word (Fig. 4, Col. 3 lines 50-59, Col. 4 lines 33-37, where register 45 comprises a reference to counter 40 and is used in determining the control and address bits to enable particular rows of the matrix).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

24. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Baddiley (US 4,852,065) as applied to **claim 9** above, and further in view of Kim et al. (US 6,781,898 B2).

25. Consider **claim 11**, Baddiley discloses a memory according to **Claim 9**, Baddiley does not disclose what happens if a faulty row exists in the matrix, however Kim et al. does teach the following claimed features: storing information relating to a faulty row in

the matrix and wherein the shifting word pointer register (38) is arranged to be controlled to skip the faulty row in the matrix and instead point to otherwise redundant additional row of the matrix (abstract, Col. 1 lines 40-46 and Col. 2 lines 8-23).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the teachings of Kim et al. with that of Baddiley, because Kim teaches that detecting and skipping defective rows in a memory and then using an additional redundant row in its place, doing this improves memory yield and ensures proper operation of the memory (abstract, Col. 1 lines 23-46 and Col. 2 lines 8-23).

26. **Claims 20-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Baddiley (US 4,852,065) as applied to **claim 1** above, and further in view of Glover (US 5,581,773).

27. Consider **claim 20**, Baddiley discloses a memory according to **Claim 1**, but does not discuss the use of a mask register, however Glover does disclose the claimed features of: a first masking register (44) arranged to mask bits of the data to be read out of the matrix of memory cells via a bit port of the memory (Col. 4 lines 11-14 and 65-67 and Col. 10 lines 57-62).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the teachings of Glover with that of Baddiley, because Glover teaches that using the PE's and register's in the manner disclosed can exclude the need for special corner turning hardware and allow for more PE's per chip therefore yielding significantly greater implementation economies and reduce cost and complexity (Col. 1 lines 43-55 and Col. 2 lines 37-67).

28. Consider **claim 21**, Baddiley discloses a memory according to **Claim 1**, but does not discuss the use of a mask register, however Glover does disclose the claimed features of: a second masking register (46) arranged to mask bits of the data to be input to the matrix of memory cells via a bit port of the memory (Col. 4 lines 11-14 and 65-67 and Col. 10 lines 57-62).

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the teachings of Glover with that of Baddiley, because Glover teaches that using the PE's and register's in the manner disclosed can exclude the need for special corner turning hardware and allow for more PE's per chip therefore yielding significantly greater implementation economies and reduce cost and complexity (Col. 1 lines 43-55 and Col. 2 lines 37-67).

29. Consider **claim 22**, Baddiley discloses a 22 a multi-ported orthogonal data memory for effecting a data corner-turning function between a plurality of processors and location addressable data store, the memory being arranged to transfer data words comprising a plurality of data items across a word port for the data store and transfer data bits across a bit port for the processors (fig. 2, abstract, Col. 1 lines 4-30 and Col. 3 lines 20-50, where a data item is considered to be a data word or some portion of a data word.), the memory comprising: a plurality of data memory cells arranged in the form of a matrix having rows and columns, and a plurality of groups of memory cells within the matrix, **wherein** each group **is** defined across multiple rows and columns, **wherein each group relates to a different size of data item** and **wherein each group is** individually addressable to effect transfer of a data word thereto (fig. 2, Col. 3 lines 20-

58 and Col. 5 lines 1-10, where a group of memory cells can be each buffer 20 and 21 themselves or a subset of a buffer that spans multiple rows and columns and the word data that is stored in each buffer and thus each group can be used to handle words of 32-bit size or smaller based on preset values and therefore each group is related to data items of a different size.); and enabling means having dedicated strobe connections to each of the plurality of groups of memory cells and being arranged to enable selected ones of the plurality of groups of memory cells, **as determined by the size of the data items being transferred**, to read data present at their inputs or to write stored data to their outputs in a single transfer operation (Fig. 2 and 3, Col. 3 lines 20-58 and Col. 5 lines 1-10, where each buffer is selected after a determination of the size of the data items is made and the arrangement of the data in the buffer is effected by the word size. Each buffer has dedicated connections for reading out and writing in data as shown in fig. 2 and 3 and a write or read operation is considered a single transfer operation.).

Baddiley uses an array of processing elements, but does not explicitly disclose whether these processing elements are SIMD processors, however Glover does teach the use of an array of processing elements just like in Baddiley that utilize SIMD processors (Col. 1 lines 13-55 and Col. 2 lines 28-42)

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the teachings of Glover with that of Baddiley, because Glover teaches that SIMD processors are frequently used to process image data, just as the

processor array in Baddiley is designed to do, therefore being a common and well-known (Col. 1 lines 41-43).

Consider **claim 23**, as applied to **claim 1** above, Baddiley uses an array of processing elements, but does not explicitly disclose whether these processing elements are SIMD processors, however Glover does teach the use of an array of processing elements just like in Baddiley that utilize SIMD processors (Col. 1 lines 13-55 and Col. 2 lines 28-42)

It would have been obvious to one of ordinary skill in the art at the time of the invention to include the teachings of Glover with that of Baddiley, because Glover teaches that SIMD processors are frequently used to process image data, just as the processor array in Baddiley is designed to do, therefore being a common and well-known (Col. 1 lines 41-43).

Response to Arguments

30. Applicant's arguments filed 10/19/2010 have been fully considered but they are not persuasive.
31. The arguments pertaining to newly added claim limitations have been addressed in the appropriate claim rejections above.
32. The Applicant describes speed benefits that would be derived from the disclosed invention in the specification and further argues that, with respect to the 35 U.S.C. 103 rejections, Baddiley would not lead one of ordinary skill to increase the speed of data transfer speed, and thus would not instruct one of ordinary skill to group the data items according to the size of the data item. However no claim language rejected under 35

U.S.C. 103 includes any type of speed related limitation requirement and thus this argument is moot.

33. The Applicant further argues that Glover fails to teach or suggest an enabling means arranged to enable selected ones of the plurality of groups of memory cells to read data present at their inputs or to write stored data to their outputs in a single transfer operation. However Glover was merely used to disclose the use of a mask register and the use of SIMD processors as claimed in **claims 20-23** and Baddiley was used to address these argued limitations and therefore this argument is moot.

Conclusion

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-1182. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael Alsip
Examiner
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/Matt Kim/

Supervisory Patent Examiner, Art Unit 2186